UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,545	10/04/2000	Gordon Margulieux	10002222-1	1130

7590 03/24/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80528-9599

EXAMINER	
BARNES, CRYSTAL J	
ART UNIT	**PAPER NUMBER**
2121	2

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/680,545	Applicant(s) MARGULIEUX, GORDON	
	Examiner Crystal J. Barnes	Art Unit 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is an initial Office Action upon examination of the above-identified application on the merits. Claims 1-20 are pending in this application.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference number 201 (first occurrence on page 7 line 3) and "dedicated storage device 1 201-1" on page 8 lines 3-4 are not shown in figure. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: reference numbers 300 in figure 3 and 400 in figure 4 are not mentioned in the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the emulated power cycling of the emulating storage system must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities: the information pertaining to the related application (see page 1) needs to be updated. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. Claims 5 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. The term "substantially approximating" in claims 5 and 19 is a relative term which renders the claim indefinite. The term "substantially approximating" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. One of ordinary skill in the art would not know what was meant by "substantially approximating" since both "substantially" and "approximating" are broad terms.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-6 and 8-20 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,903,719 to Yamamoto.

As per claim 1, the Yamamoto reference discloses a system for providing accurate data storage emulation in a computer system, the system comprising a host computer system (see column 1 lines 17-18 and 29-30, "host computer 31, target system 34") having at least one storage system (see column 1 lines 32-33 and column 7 lines 22-27, "hard disk unit 36, trace memory unit 18, preservation memory unit 19"); an emulating computer (see column 5 lines 21-22 and 30-32, "emulator apparatus 33") in communication ("communication cable 32, probe 35") with said host computer system ("host computer 31, target system 34"); and an emulating storage system (see column 5 lines 30-33 and 45-55, "emulation memory unit 12, preservation memory unit 19") in communication ("system bus 13") with said

emulating computer ("microcomputer 11") dedicated to emulation of an operation of at least one of said at least one storage systems (see column 7 lines 43-49, "restoration of history execution").

As per claim 2, the Yamamoto reference discloses said emulating storage system is disposed within an enclosure housing said emulating computer (see figure 3 and column 5 lines 45-55 and column 7 lines 22-24, "emulator apparatus 33").

As per claim 3, the Yamamoto reference discloses said emulating storage system is located externally to an enclosure housing said emulating computer (see figure 5 and column 7 lines 22-27, "emulating apparatus 33").

As per claim 4, the Yamamoto reference discloses at least on additional emulating storage system (see column 5 lines 45-55 and column 7 lines 39-43, "RAM data area, data-register area, control-register area, memory-address/data area").

As per claim 5, the Yamamoto reference discloses said emulating storage system (see column 6 lines 1-9, "RAM-data area 21") includes operating characteristics substantially approximating operating characteristics of said at least one storage system of said host computer ("RAM unit employed in the target system 34").

As per claim 6, the Yamamoto reference discloses means for preserving data (see column 5 lines 47-55, "RAM-data area 21") stored in said emulating storage system ("preservation memory unit 19") during emulated power cycling "relative-bus-cycle area 22") of said emulating storage system ("preservation memory unit 19").

As per claim 8, the Yamamoto reference discloses said emulating storage system (see column 5 lines 45-46, "preservation memory unit 19") substantially excludes data pertaining to internal operation of said emulating computer (see column 5 lines 30-33, "emulation memory unit 12").

As per claim 9, the rejection of claim 1 is incorporated and further claim 9 contains limitations recited in claim 1; therefore claim 9 is rejected under the same rationale as claim 1.

As per claim 10, the rejection of claim 8 is incorporated and further claim 10 contains limitations recited in claim 8; therefore claim 10 is rejected under the same rationale as claim 8.

As pr claim 11, the rejection of claim 2 is incorporated and further claim 11 contains limitations recited in claim 2; therefore claim 11 is rejected under the same rationale as claim 2.

As per claim 12, the rejection of claim 3 is incorporated and further claim 12 contains limitations recited in claim 3; therefore claim 12 is rejected under the same rationale as claim 3.

As per claim 13, the Yamamoto reference discloses further comprising the step of dedicating each of a plurality of emulating storage devices (see column 5 lines 45-55, "RAM data area 21, data-register area 23, control-register area 24") to a separate one of said at least one storage devices ("RAM unit, data registers of the CPU, control registers of the CPU) native to said host computer system ("target system 34").

As per claim 14, the Yamamoto reference discloses further comprising the step of emulating a succession (see column 5 lines 45-55, "relative bus cycles") of said at least one storage device ("RAM unit, data registers of the CPU, control registers of the CPU) native to said host computer system ("target system 34") employing a succession ("relative-bus-cycles area 22") of said plurality of dedicated emulating storage devices ("RAM data area 21, data-register area 23, control-register area 24").

As per claim 15, the Yamamoto reference discloses further comprising the step of preserving data (see column 5 lines 45-55, "preservation memory unit 19")

stored in said plurality of dedicated emulating storage devices ("RAM data area 21, data-register area 23, control-register area 24") while said succession ("relative bus cycles") of said at least one storage devices ("RAM unit, data registers of the CPU, control registers of the CPU) native to said host computer system ("target system 34") is emulated.

As per claim 16, the Yamamoto reference discloses a system for emulating an operation of at least one storage device adapted for operation with a host computer system, the system comprising means for dedicating an emulating storage device (see column 5 lines 45-55, "RAM data area 21, data-register area 23, control-register area 24") to each of said at least one storage devices ("RAM unit, data registers of the CPU, control registers of the CPU) adapted for operation with said host computer system ("target system 34"), thereby establishing at least one dedicated emulating storage device ("RAM data area 21, data-register area 23, control-register area 24"); means for coupling said at least one dedicated emulating storage device ("RAM data area 21, data-register area 23, control-register area 24") to said host computer ("target system 34") via an intelligent interface (see columns 1-2 lines 66-2, "probe 35"); and means for monitoring an

operation (see column 5 lines 56-62, "step execution function") of said at least one dedicated emulating storage device ("emulating apparatus 33").

As per claim 17, the Yamamoto reference discloses said monitoring means comprises means for diagnosing a fault condition (see column 5 lines 56-62, "debug operation") among said at least one dedicated emulating storage devices ("emulating apparatus 33").

As per claim 18, the Yamamoto reference discloses said monitoring means further comprises means for performing diagnostic operations (see column 6 lines 2-8, "undo mode") in response to said diagnosed fault condition (see column 5 lines 56-62, "debug operation").

As per claim 19, the Yamamoto reference discloses said means for dedicating comprises selecting said at least one dedicated emulating storage device (see column 5 lines 45-55, "RAM data area 21, data-register area 23, control-register area 24") having operating characteristics substantially approximating operating characteristics of said at least one storage device ("RAM unit, data registers of the CPU, control registers of the CPU) adapted for operation with said host computer system ("target system 34").

As per claim 20, the Yamamoto reference discloses said intelligent interface is a computer (see columns 1-2 lines 66-2, "probe 35").

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,903,719 to Yamamoto in view of logical reasoning.

As per claim 7, the Yamamoto reference discloses said at least one storage system comprises a hard disk drive unit (see column 7 lines 61-65, "hard-disk unit 36") having a storage capacity and said emulating storage system ("preservation memory unit 19") comprises a hard disk drive having a storage capacity substantially equal to said storage capacity of said hard disk drive ("hard-disk unit 36").

The Yamamoto reference does not expressly disclose said emulating storage system comprises a hard disk drive having a storage capacity substantially equal to said storage capacity of said hard disk drive.

However, it would have been logically to one of ordinary skill in the art to modify the third embodiment taught by Yamamoto to include an additional embodiment that incorporated a hard disk unit to back up and not reduce the preservation memory unit. As a result, both the hard disk unit and the preservation memory unit would have the same capacity.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make a variety of changes and modifications of the embodiments without departing from the spirit and scope of the Yamamoto reference.

One of ordinary skill in the art would have been motivated to incorporate a hard disk unit to back up the preservation memory unit so that both the hard disk unit and the preservation memory unit would have the same capacity.

Conclusion

13. No claims are allowed.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to emulating memory/storage devices in general:

USPN 6,578,127 B1 to Sinclair

USPN 6,574,588 B1 to Shapiro et al.

USPN 6,571,356 B1 to Mehr et al.

USPN 6,480,845 B1 to Egolf et al.

USPN 6,063,131 to Yoshida

USPN 6,009,261 to Scalzi et al.

USPN 5,873,129 to Bealkowski

USPN 5,838,952 to Okano et al.

USPN 5,832,251 to Takahashi

USPN 5,025,364 to Zellmer

JPPN 4-289470 A to KAWAI

JP Pub. No. 11-175366 A to CHIBA

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 703.306.5448. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anil Khatri can be reached on 703.305.0282. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cjb
15 March 2004

Wilbert L. Starks, Jr.
Primary Examiner
Art Unit - 2121